IN THE CLAIMS

A detailed listing of all claims that are, or were, in the present application, irrespective of whether the claim(s) remains under examination in the application are presented below. The claims are presented in ascending order and each includes one status identifier. Those claims not cancelled or withdrawn but amended by the current amendment utilize the following notations for amendment: 1. deleted matter is shown by strikethrough for six or more characters and double brackets for five or less characters; and 2. added matter is shown by underlining.

1. (Original) A wireless spread spectrum communication system for transmitting data comprising:

a plurality of end point transmitters transmitting data via a frequency hopped spread spectrum signal, the transmitting signal being sent without the benefit of frequency stabilization; and

at least one receiver responsive to the frequency hopping spread spectrum signals, each receiver including:

a correlator that samples at least a first portion of a preamble of the signal and correlates the portion of the preamble with a known preamble pattern to determine a probability of correlation; and

a signal processor that applies an algorithm to the signal in response to the probability of correlation to track a narrowband frequency of the signal based on at least a second portion of the preamble and to decode data encoded within the signal subsequent to the preamble.

2. (Original) The system of claim 1 wherein the signal processor is a digital signal processor (DSP).

3. (Original) The system of claim 1 wherein the algorithm used to identify the narrowband frequency of the signal and to decode the data within the signal is a Fast Fourier Transform (FFT).

4. (Original) The system of claim 3 wherein the FFT algorithm operates on sampled data to produce multiple bins, each bin corresponding to a different narrowband frequency within the signal.

5. (Original) The system of claim 4 wherein the FFT algorithm sums a plurality of chip values in each bin against expected chip values to determine a bin having a highest value as the narrowband frequency containing the encoded data signal.

6. (Original) The system of claim 3 wherein a strength of the signal supplied to the correlator is evaluated and if the strength of the signal supplied to the correlator is strong enough to perform a decode of the data encoded within the signal subsequent to the preamble, the signal processor does not use the FFT algorithm to decode the data encoded within the signal subsequent to the preamble.

7. (Original) The system of claim 1 wherein the correlator samples data using a 12 bit analog-to-digital converter connected to a Received Signal Strength Indicator (RSSI).

8. (Original) The system of claim 7 further comprising:

a mixer that receives the signal and mixes the signal with a base signal to produce an intermediate frequency that is supplied as the signal to the correlator and the signal processor.

9. (Original) The system of claim 1 wherein the correlator samples over at least sixty-six percent (66%) of a wideband frequency for the signal.

10. (Original) The system of claim 1 wherein the correlator is implemented using the digital signal processor.

11. (Currently Amended) The system of claim 10 wherein the digital signal processor is supplied with two sampled inputs, a first sampled input from an analog-to-digital converter oper[[r]]ating at a first speed and a second sampled input from an analog-to-digital converter operating at a second speed, where the second speed is slower than the first speed.

12. (Original) The system of claim 11 further comprising a received signal strength indicator (RSSI) detector circuit operably connected to an input to the second analog-to-digital converter.

13. (Original) The system of claim 1 wherein the receiver further comprises:

a switchable front-end amplifier that operably receives the signals and selectively attenuates the signals based on signal strength; and

a linear detector operably coupled to an output of the front-end amplifier and to an input of the correlator.

14. (Original) The system of claim 1 wherein the signal is sampled during the decoding of the encoded data at a rate less than twice a data rate of the encoded data.

15. (Original) The system of claim 1 wherein the signal is sampled during the decoding of the encoded data at unequal intervals.

16. (Original) The system of claim 1 wherein the signal is sampled during the decoding of the encoded data in a middle portion of a bit period without sampling at edge portions of the bit period.

17. (Currently Amended) The system of claim 16 wherein the middle portion represents seventy five percent (75%) or less of the bit period.

18. (Currently Amended) The system of claim 1 wherein the correlator operates to establish both a bit synchronization and a frame synchronization for the encoded data in the signal.

19. (Original) The system of claim 1 wherein the signal processor initiates the algorithm only when the probability of correlation is greater than a threshold value.

20. (Original) The system of claim 19 wherein the threshold value is established based on an average of a predetermined number of raw input bits.